CLAIMS

What is claimed:

1. A system for processing applications, the system comprising:

a plurality of processor nodes with each processor node comprising:

a processing element configured to execute at least one of the applications;

a software extensible device configured to provide additional instructions to a set of standard instructions for the processing element; and

a communication interface configured to communicate with other processor nodes; and

a plurality of links interconnecting the processor nodes.

2. The system of claim 1 wherein each one of the processor nodes is on a separate chip.

3. The system of claim 1 wherein at least some of the processor nodes are on the same chip.

4. The system of claim 1 wherein the plurality of the processor nodes are configured in an array.

5. The system of claim 1 wherein the software extensible device comprises an instruction set extension fabric.

6. The system of claim 1 wherein the software extensible device comprises a programmable logic device.

7. The system of claim 1 wherein the communication interface is configured to communicate using shared memory.

8. The system of claim 1 wherein the communication interface is configured to communicate using message passing.

9. The system of claim 1 wherein the communication interface is configured to communicate using channels between the processor nodes.

10. The system of claim 9 wherein the communication interface is configured to perform time division multiplexing using the channels between the processor nodes.

11. The system of claim 9 wherein the communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes.

12. The system of claim 1 wherein the communication interface comprises a processor network interface.

13. The system of claim 1 wherein the communication interface comprises a processor network switch.

14. The system of claim 1 wherein the communication interface comprises a standard input/output interface.

15. The system of claim 1 wherein the communication interface comprises an interface module configured to communicate between processor nodes on different chips.

16. The system of claim 1 wherein the communication interface comprises a multiplexer/demultiplexer.

17. The system of claim 1 wherein at least one of the processor nodes is different from the other processor nodes.

18. A method for a system with multiple processor nodes, the method comprising:

executing an application in at least one processing element in a plurality of the processor nodes;

providing an additional instruction to a set of standard instructions for the processing element using at least one software extensible device in the plurality of the processor nodes; and

communicating between the processor nodes using at least one communication interface in a plurality of the processor nodes.

19. The method of claim 18 wherein communicating between the processor nodes comprises using shared memory.

20. The method of claim 18 wherein communicating between the processor nodes comprises using message passing.

21. The method of claim 18 wherein communicating between the processor nodes comprises using channels between the processor nodes.

22. The method of claim 21 wherein using the channels between the processor nodes further comprises performing time division multiplexing with the channels.

23. The method of claim 21 wherein using the channels between the processor nodes further comprises performing spatial division multiplexing with the channels.

24. The method of claim 18 further comprising compiling the application.

25. The method of claim 18 further comprising loading the application into one of the plurality of the processor nodes.

26. The method of claim 18 further comprising configuring one of the processor nodes to select between an interface module and a standard input/output interface based on a neighboring device.

27. A method for routing a packet in a plurality of processor nodes, the method comprising:

receiving the packet into one of the processor nodes with a software extensible device;

comparing a first destination address of the packet with a second destination address of the one of the processor nodes;

processing the packet in the one of the processor nodes in response to the first destination address matching the second destination address;

determining an egress port in the one of the processor nodes in response to the first destination address not matching the second destination address; and

routing the packet to the egress port.

28. The method of claim 27 wherein determining the egress port further comprises using an identification of the packet with a static table of the egress ports.

29. The method of claim 27 wherein determining the egress port further comprises:

determining whether a destination of the packet is near the one of the processor nodes; and

determining the egress port based on a near table of the egress ports.

30. The method of claim 27 wherein determining the egress port further comprises:

determining whether a destination of the packet is far from the one of the processor nodes; and

determining the egress port based on a far table of the egress ports.